FIG.1

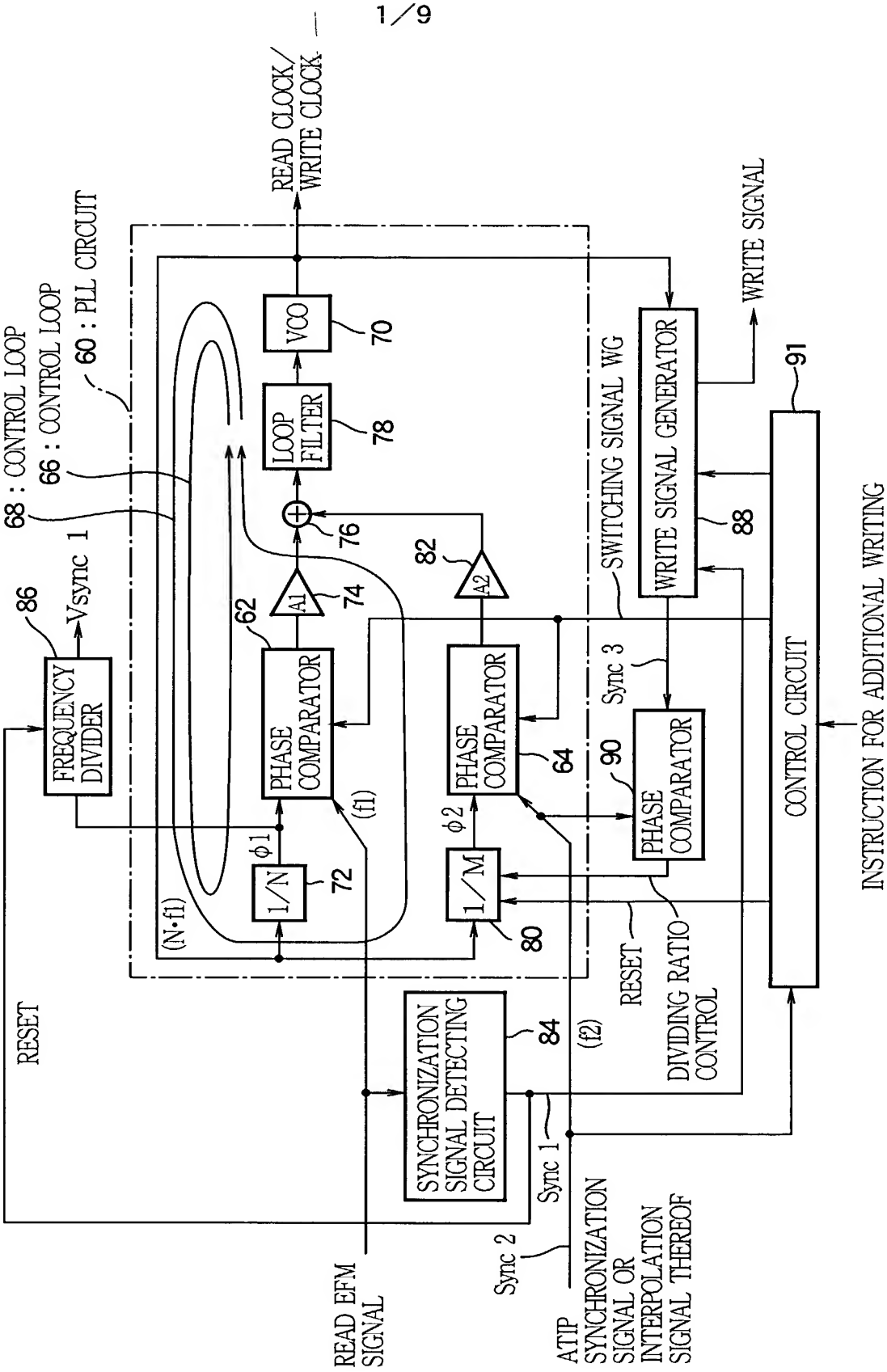

READ CLOCK/
WRITE CLOCK
60 : PLL CIRCUIT
66 : CONTROL LOOP
68 : CONTROL LOOP
VCO
70
LOOP
FILTER
78
76
A1
74
A2
82
62
PHASE
COMPARATOR
64
PHASE
COMPARATOR
90
PHASE
COMPARATOR
φ1
1/N
72
φ2
1/M
80
(N·f1)
(f1)
(f2)
FREQUENCY
DIVIDER
86
Vsync 1
SWITCHING SIGNAL WG
Sync 3
WRITE SIGNAL GENERATOR
88
WRITE SIGNAL
91
CONTROL CIRCUIT
INSTRUCTION FOR ADDITIONAL WRITING
RESET
RESET
DIVIDING RATIO
CONTROL
SYNCHRONIZATION
SIGNAL DETECTING
CIRCUIT
84
Sync 1
Sync 2
READ EFM
SIGNAL
ATIP
SYNCHRONIZATION
SIGNAL OR
INTERPOLATION
SIGNAL THEREOF

FIG.2

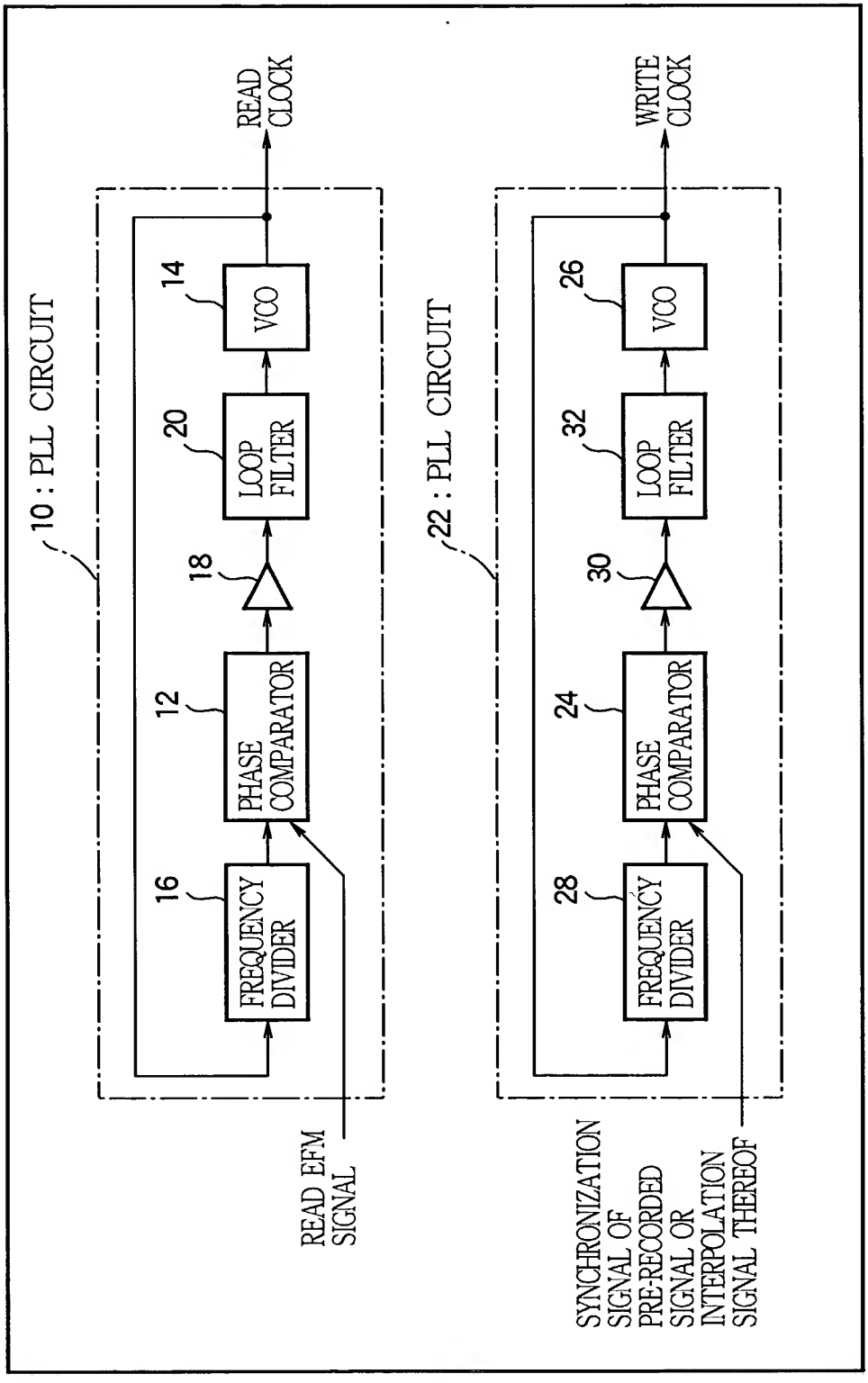

10 : PLL CIRCUIT
22 : PLL CIRCUIT
READ CLOCK
WRITE CLOCK
VCO
LOOP FILTER
PHASE COMPARATOR
FREQUENCY DIVIDER
14
20
18
12
16
26
32
30
24
28
READ EFM SIGNAL
SYNCHRONIZATION SIGNAL OF PRE-RECORDED SIGNAL OR INTERPOLATION SIGNAL THEREOF

FIG.3

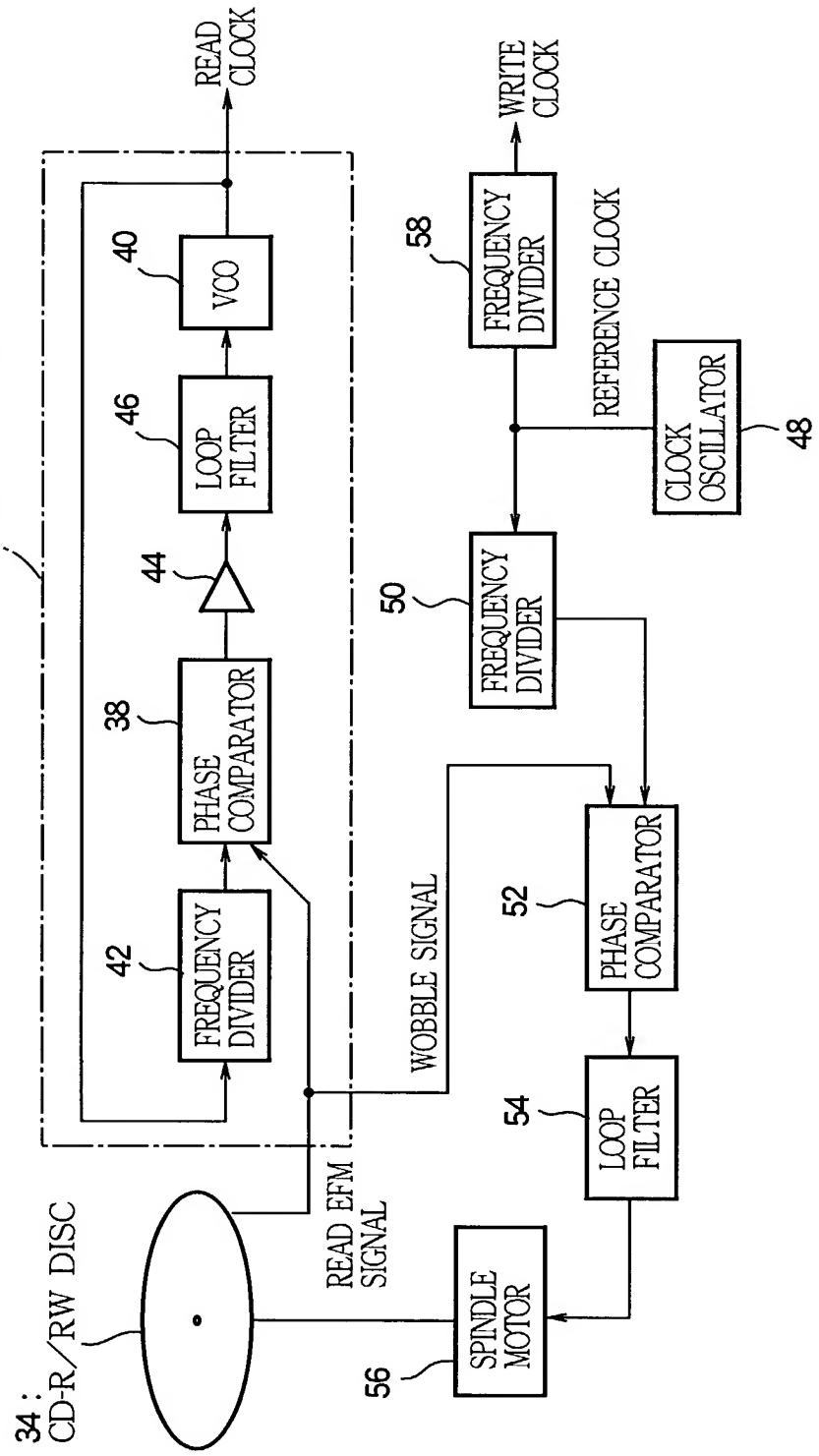

READ CLOCK
WRITE CLOCK
36 : PLL CIRCUIT
VCO
40
LOOP FILTER
46
44
PHASE COMPARATOR
38
FREQUENCY DIVIDER
42
FREQUENCY DIVIDER
58
FREQUENCY DIVIDER
50
REFERENCE CLOCK
CLOCK OSCILLATOR
48
WOBBLE SIGNAL
PHASE COMPARATOR
52
LOOP FILTER
54
SPINDLE MOTOR
56
READ EFM SIGNAL
34 : CD-R/RW DISC

FIG.4

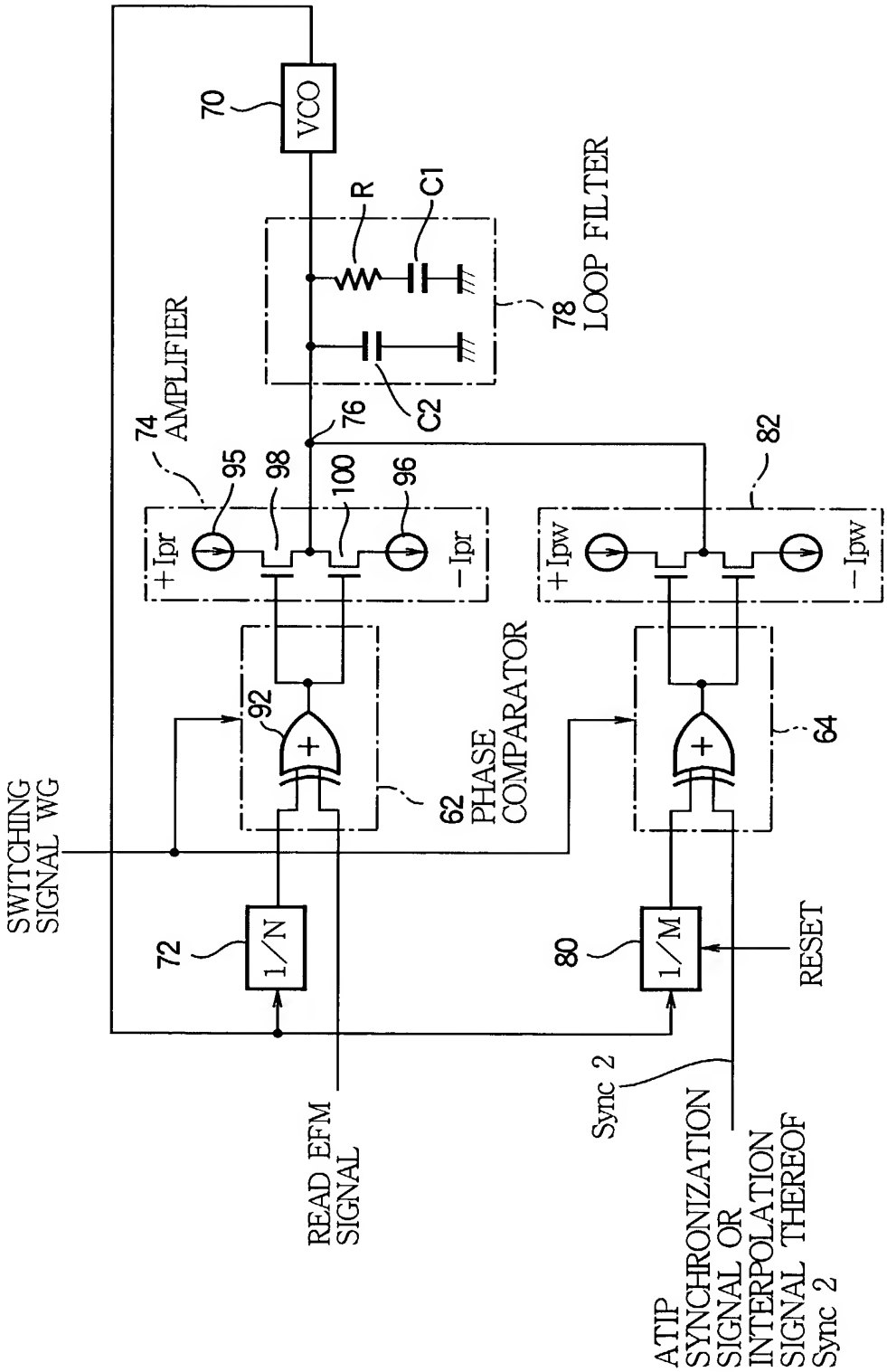

70
VCO
R
C1
78
LOOP FILTER
C2
76
74
AMPLIFIER
95
98
100
96
82
+Ipr
−Ipr
+Ipw
−Ipw
92
62
PHASE
COMPARATOR
64
SWITCHING
SIGNAL WG
72
1/N
80
1/M
RESET
READ EFM
SIGNAL
Sync 2
ATIP
SYNCHRONIZATION
SIGNAL OR
INTERPOLATION
SIGNAL THEREOF
Sync 2

FIG.5

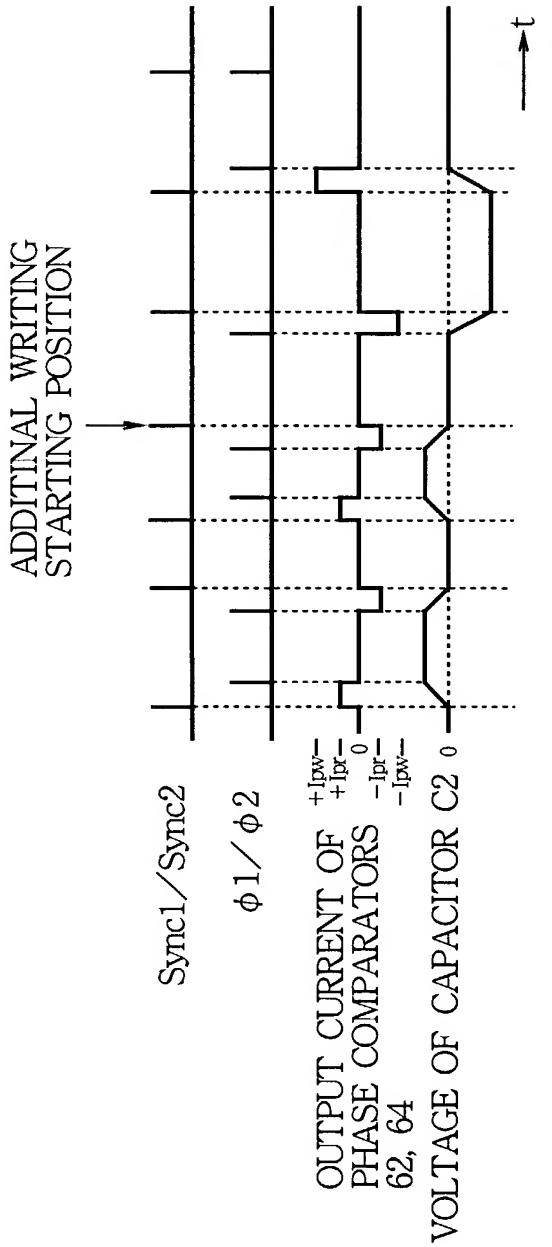

ADDITINAL WRITING
STARTING POSITION
Sync1/Sync2
φ1/φ2
OUTPUT CURRENT OF
PHASE COMPARATORS
62, 64
VOLTAGE OF CAPACITOR C2
+Ipw
+Ipr
0
-Ipr
-Ipw
0
t

FIG.6

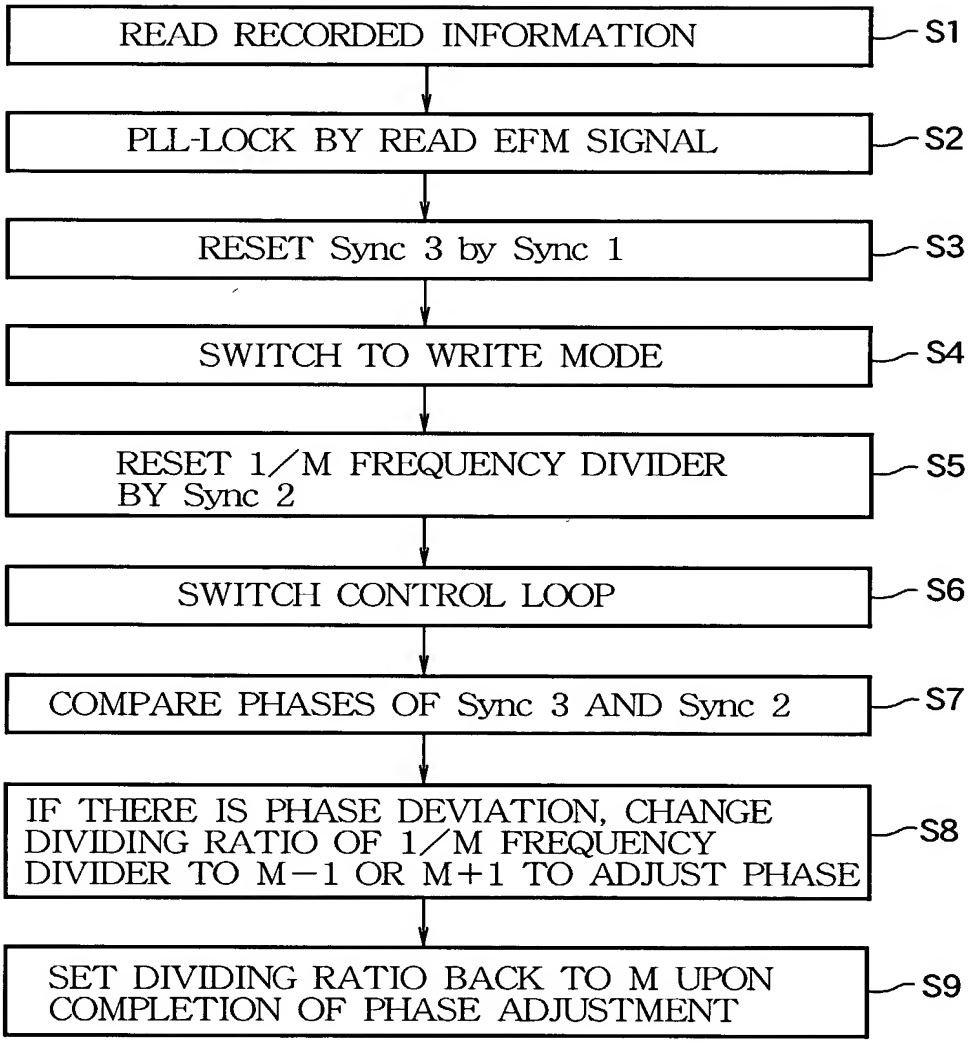

READ RECORDED INFORMATION
S1
PLL-LOCK BY READ EFM SIGNAL
S2
RESET Sync 3 by Sync 1
S3
SWITCH TO WRITE MODE
S4
RESET 1/M FREQUENCY DIVIDER BY Sync 2
S5
SWITCH CONTROL LOOP
S6
COMPARE PHASES OF Sync 3 AND Sync 2
S7
IF THERE IS PHASE DEVIATION, CHANGE DIVIDING RATIO OF 1/M FREQUENCY DIVIDER TO M−1 OR M+1 TO ADJUST PHASE
S8
SET DIVIDING RATIO BACK TO M UPON COMPLETION OF PHASE ADJUSTMENT
S9

FIG.7

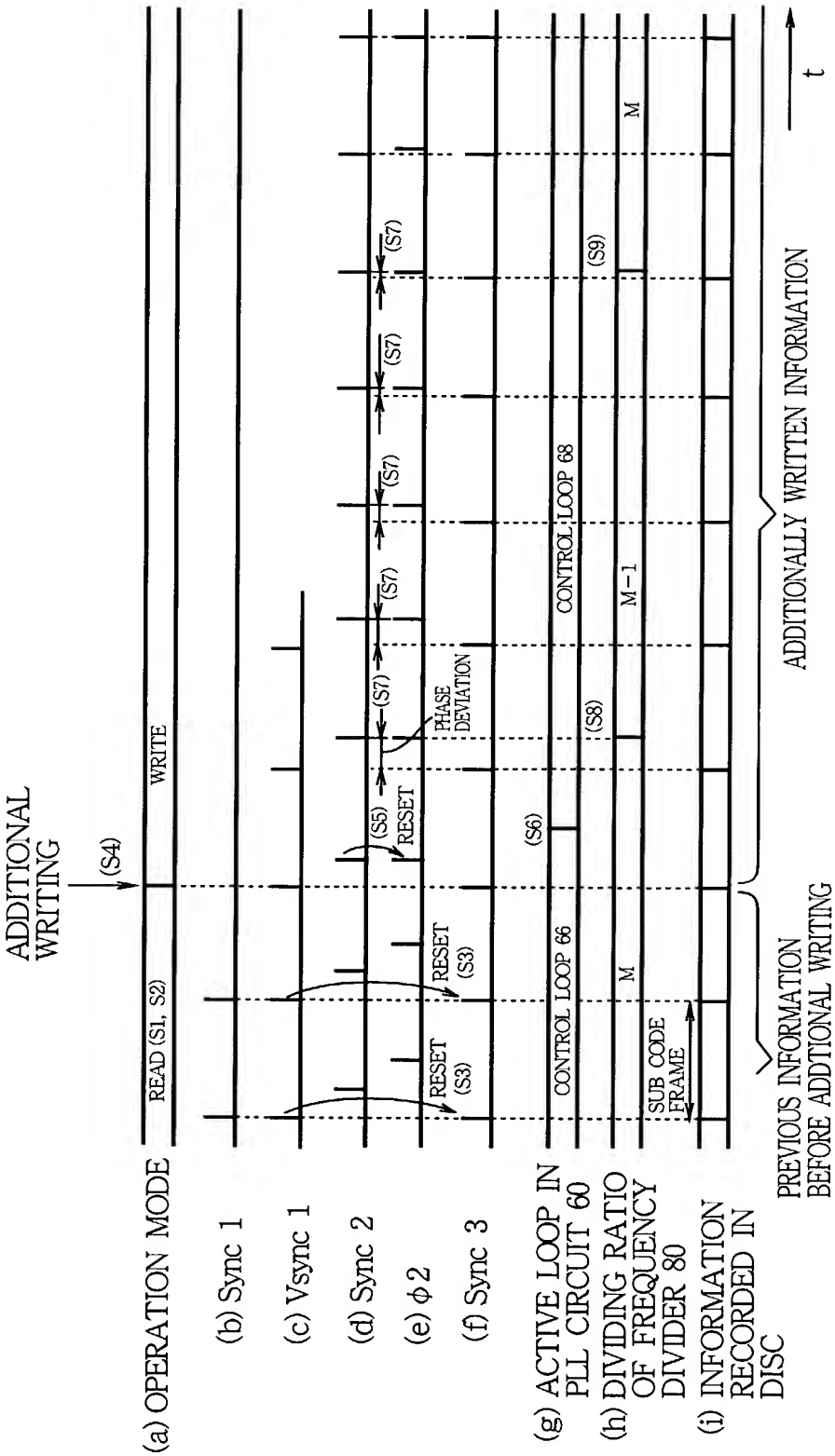

ADDITIONAL WRITING
(S4)
(a) OPERATION MODE
READ (S1, S2)
WRITE
(b) Sync 1
(c) Vsync 1
(d) Sync 2
(S5)
RESET
(S7)
PHASE DEVIATION
(e) φ2
RESET (S3)
(f) Sync 3
RESET (S3)
(S6)
(g) ACTIVE LOOP IN PLL CIRCUIT 60
CONTROL LOOP 66
CONTROL LOOP 68
(S8)
(S9)
(h) DIVIDING RATIO OF FREQUENCY DIVIDER 80
M
M-1
M
SUB CODE FRAME
(i) INFORMATION RECORDED IN DISC
PREVIOUS INFORMATION BEFORE ADDITIONAL WRITING
ADDITIONALLY WRITTEN INFORMATION
t

FIG.8

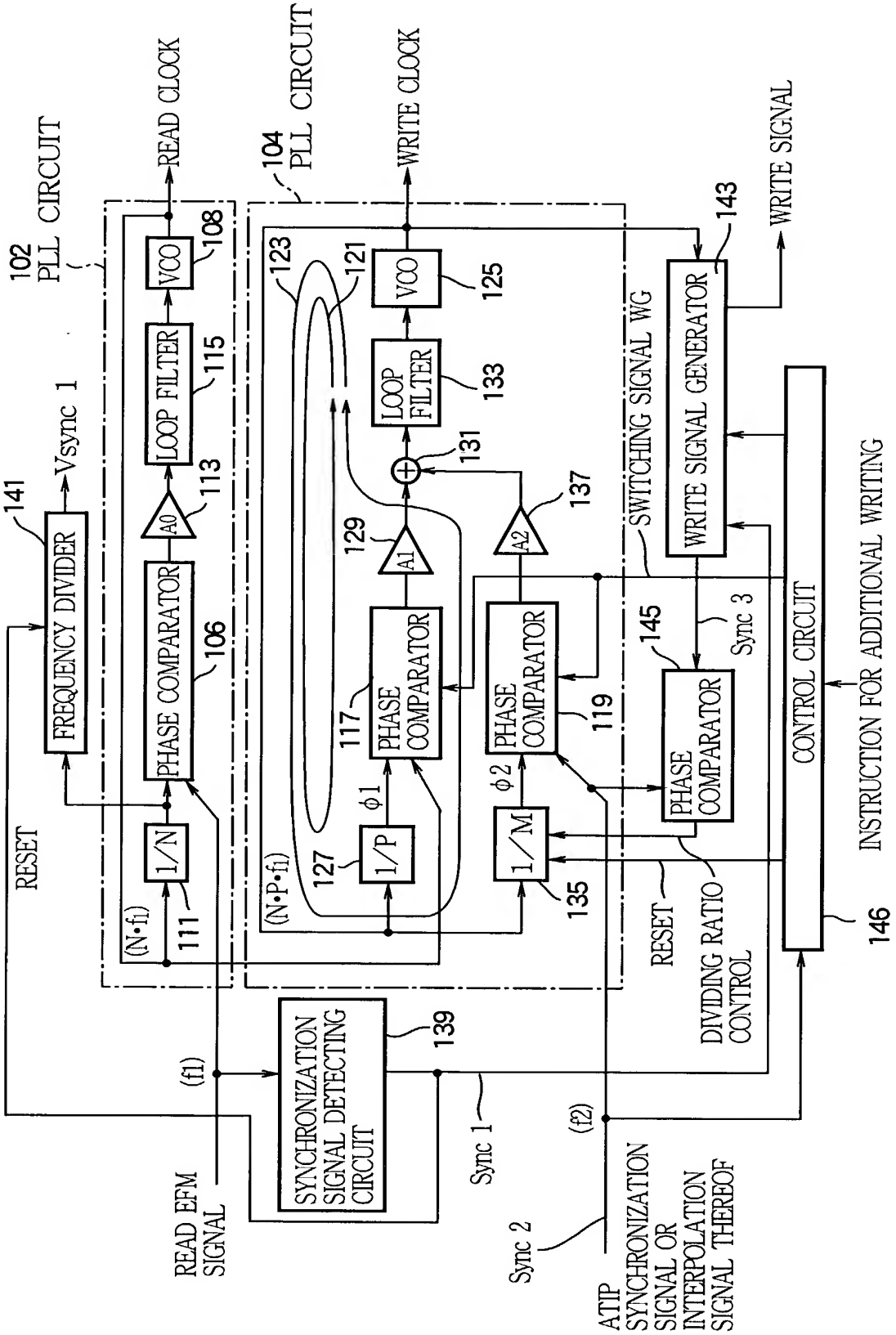
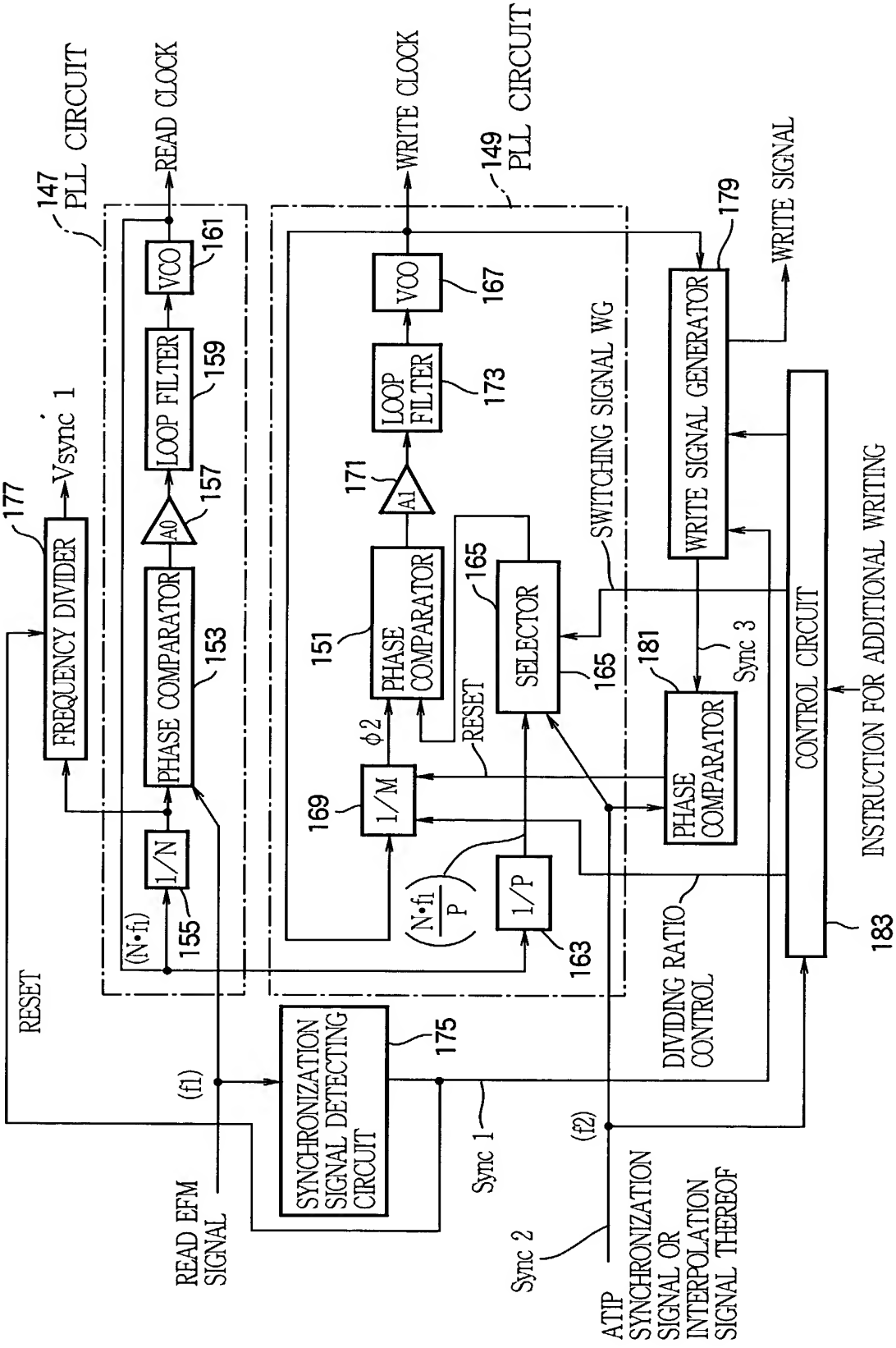

102
PLL CIRCUIT
READ CLOCK
104
PLL CIRCUIT
WRITE CLOCK
WRITE SIGNAL
141
Vsync 1
FREQUENCY DIVIDER
RESET
PHASE COMPARATOR
106
A0
113
LOOP FILTER
115
VCO
108
123
121
VCO
125
LOOP FILTER
133
131
A1
129
A2
137
SWITCHING SIGNAL WG
WRITE SIGNAL GENERATOR
143
1/N
111
(N•fi)
1/P
φ1
127
PHASE COMPARATOR
117
(N•P•fi)
φ2
1/M
135
PHASE COMPARATOR
119
PHASE COMPARATOR
145
Sync 3
CONTROL CIRCUIT
INSTRUCTION FOR ADDITIONAL WRITING
146
RESET
DIVIDING RATIO CONTROL
(f1)
READ EFM SIGNAL
SYNCHRONIZATION SIGNAL DETECTING CIRCUIT
139
Sync 1
(f2)
Sync 2
ATIP SYNCHRONIZATION SIGNAL OR INTERPOLATION SIGNAL THEREOF

FIG.9


147
PLL CIRCUIT
READ CLOCK
149
PLL CIRCUIT
WRITE CLOCK
FREQUENCY DIVIDER
177
Vsync 1
PHASE COMPARATOR
153
LOOP FILTER
159
VCO
161
1/N
155
(N•fi)
A0
157
PHASE COMPARATOR
151
LOOP FILTER
173
VCO
167
1/M
169
φ2
A1
171
SELECTOR
165
SWITCHING SIGNAL WG
WRITE SIGNAL GENERATOR
179
WRITE SIGNAL
RESET
RESET
1/P
163
(N•fi/P)
PHASE COMPARATOR
181
Sync 3
CONTROL CIRCUIT
183
INSTRUCTION FOR ADDITIONAL WRITING
DIVIDING RATIO CONTROL
SYNCHRONIZATION SIGNAL DETECTING CIRCUIT
175
(f1)
(f2)
Sync 1
Sync 2
READ EFM SIGNAL
ATIP SYNCHRONIZATION SIGNAL OR INTERPOLATION SIGNAL THEREOF